CLOCK SYNCHRONIZATION CIRCUIT AND METHOD

Abstract

A clock synchronization circuit for generating an output clock signal that is in synchronization with a reference clock signal and a method embodying the principle of operation of the circuit are disclosed. The circuit has a programmable delay element and a phase detector. Synchronization is reached when the phase difference between the two clock signals is less than a predetermined value. The programmable delay element is coupled to the reference clock signal for introducing an adjustable delay in the reference clock signal to produce the output clock signal. By increasing the adjustable delay, the output clock signal becomes increasingly closer to being in synchronization with the reference clock signal. The phase detector is coupled to the reference clock signal and the output clock signal for detecting the phase difference between the two clock signals. The adjustable delay is increased until synchronization is obtained.